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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,564	TODD ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50 and 55-80* is/are pending in the application.

4a) Of the above claim(s) *3,4 and 47-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-46 and 55-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/9/03;4/9/04;9/13/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election with traverse of Species I, i.e., claims 1-2, 5-21, 26-50 and 55-80 in the reply filed on November 15, 2004 is acknowledged. The traversal is on the ground(s) that "Claims 22-25 are also readable on Species I because the specification discloses that Si-N may be amorphous..." This is found persuasive. Accordingly, claims 22-25 are treated as being read on Species I.

2. Because applicants did not distinctly and specifically point out the supposed errors in the restriction requirement for Species II and III, i.e., claims 3 and 4 reads on Species II and III, the election with respect to Species II and III has been treated as an election without traverse (MPEP § 818.03(a)). Accordingly, Claims 3 and 4 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on November 15, 2004.

3. Claims 47-50 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on June 27, 2003.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-3, 5-46 and 55-80 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of U.S. Patent No. 6,821,825 in view of Toraguchi et al. (US/6,161,498).

Re claims 1-3, 5-46, and 55-80, the claimed subject matter of the instant application essentially claimed in claims 1-25 of U.S. Patent 6,821,825. The claimed limitations include introducing trisilane to a chamber, wherein the chamber contains a substrate; depositing a continuous amorphous Si-containing film having a thickness of less than about 100 A and a surface area of about one square micron or larger onto the substrate by thermal chemical vapor deposition (see Claims 1 and 7); wherein the substrate comprises a non-single crystal material (see Claim 8); wherein the Si-containing film is deposited directly onto the non-single crystal layer and the non-single crystal layer is selected from the group consisting of silicon oxide, metal oxide, metal silicate, silicon oxynitride and silicon nitride (see Claims 16 and 17); wherein the Si-containing film has a thickness non-uniformity of about 15% or less for a mean film thickness in the range of 50 A to 99 A, and a thickness non-uniformity of about 20% or less for a mean film thickness of less than 50 A (see Claims 8 and 9); wherein the depositing is conducted at a temperature in the range of about 450°C to about 650°C (see Claim 5); wherein the depositing is conducted in or near a mass transport limited regime for trisilane (see Claim 1). Furthermore, the surface roughness and the forming the quantum dot is within the scope of U.S. Patent No.

6,821,825 since the claimed subject matter of U.S. Patent No. 6,821,825 claimed all the necessary conditions to achieve the claimed result of the instant application.

However, Ikoma et al. do not specifically disclose using 300 cm^2 or grater wafer (substrate) to deposit the Si-containing film.

U.S. Patent No. 6,821,825 does not claim a larger wafer, i.e., having diameter 300 mm (12 inches), i.e., larger than 300 cm^2 as claimed, in order to deposit thin films for fabrication of IC devices (see Toraguchi et al. Col. 2, lines 24-31; Col. 6, lines 1-13). As known in the art, larger wafer size provides enough surface area to fabricate several hundred individual IC devices on a single substrate assembly and can achieve greater process control and precision in the batch-processing during fabrication of the semiconductor devices (see Goodman page 1 Paragraph [0005]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Ikoma et al. reference with large size wafer i.e., larger that 300 cm^2 size as taught by Toraguchi et al. because larger wafer size provides enough surface area to fabricate several hundred individual IC devices on a single substrate assembly and can achieve greater process control and precision in the batch-processing during fabrication of the semiconductor devices.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikoma et al., Growth of Si/3C-SiC/Si(100) hetrostructures by pulsed supersonic free jets, *Applied Physics Letters*, Volume 75, No. 25, Pp. 3977-3979, December 1999.

Re claim 69, Ikoma et al. disclose a method for depositing a thin film, comprising: introducing a gas comprising trisilane to a chamber (see Abstract); wherein the chamber contains a substrate having a predetermined surface are and a substrate surface roughness (see Page 3977, Col. 1); establishing trisilane chemical vapor deposition conditions in the chamber (i.e., CVD chamber See Page 3977, Col. 2) ; and depositing a Si-containing (i.e., Si-C, epi-Si or poly-Si film) film onto the substrate, the Si-containing film having a thickness in the range of 30 – 90 angstroms (i.e., within the overlap claimed range of 10 - 150 angstroms) and a film surface roughness that is greater than the substrate surface roughness by an amount of about 4 angstrom rms (i.e., within the claimed rage of 5 Å rms or less), over a surface area of about 25 micron square (i.e., within the claimed range of one square micron or greater) at predetermined chamber pressure. Although Ikoma et al. do not specifically disclose the claimed chamber pressure range, the claimed pressure that is 1 torr to 100 torr is typical chamber pressure and one of ordinary

skill in the art would have been motivated to optimize chamber pressure by using routine experimentation in order to achieve the desired deposition environment (i.e., the general condition that disclosed by the combination of Ikoma et al.).

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the substrate temperature prior deposition of the film, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed pressure range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

8. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US/5,849,601).

Re claim 70, Yamazaki discloses a method for depositing a thin film, comprising: introducing trisilane to a chamber, wherein the chamber contains a substrate having a predetermined surface area; and depositing a continuous amorphous Si-containing film having a thickness of less than about 500 angstroms and a surface area of about one square micron or

larger onto the substrate by thermal chemical vapor deposition (i.e., LPCVD that also has heating process) (see Col. 13, lines 5-10).

Furthermore, the thickness 100 angstroms or less of the amorphous Si-containing layer can be achieved within the level of ordinary skill in the art in order to optimize the size of the device. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

9. Claims 76 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (US/6,385,020).

Re claim 76, Shin et al. disclose a method for depositing a thin film, comprising: introducing trisilane to a CVD chamber (see Col. 11, line 60 –Col. 12 line 5), wherein the chamber contains a substrate (Figs. 6 and 7); depositing a continuous amorphous Si-containing film having a thickness of less than about 250 Å and a surface area of about one square micron or larger onto the substrate (See Figs. 6 and 7) by thermal chemical vapor deposition; and

annealing the amorphous Si-containing film to form hemispherical grained silicon (see Figs. 6 and 7; Col. 11, line 46 –Col. 12 line 5).

Furthermore, the thickness 100 angstroms or less of the amorphous Si-containing layer can be achieved within the level of ordinary skill in the art in order to optimize the size of the device. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

10. Claims 77-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (US/5,591,494).

Re claim 77, Sato et al. disclose a method for depositing a thin film, comprising: introducing trisilane and a nitrogen precursor to a chamber (see Col. 1, line 64 – Col. 2, line 6), wherein the chamber contains a substrate ; depositing a continuous amorphous Si-containing film having a predetermined thickness of and a surface area of about one square micron or larger onto the substrate by thermal chemical vapor deposition (see Col. 1, line 64 – Col. 4, line 33).

Furthermore, the thickness 100 angstroms or less of the amorphous Si-containing layer can be achieved within the level of ordinary skill in the art in order to optimize the size of the device. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claim 78, as applied to claim 77 above, Sato et al. disclose all the claimed limitations including the limitation wherein the trisilane is introduced to the chamber in one or more pulses (i.e., the trisilan is injected in the chamber as the form of pulse during PECVD process) (see Col. 1, line 64 – Col. 4, line 33).

Re claim 79, as applied to claim 78 above, Sato et al. disclose all the claimed limitations including the limitation wherein the nitrogen precursor is atomic nitrogen (see Col. 1, line 64 – Col. 4, line 33).

Re claim 80, as applied to claim 78 above, Sato et al. disclose all the claimed limitations including the limitation wherein the depositing is conducted at a temperature in the range of about 300°C to about 400°C (i.e., outside of the claimed range of 450°C to about 650°C) (see Col. 1, line 64 – Col. 4, line 33).

Although Sato et al. deposition temperature is outside of the claimed temperature range that is 450°C to about 650°C, one of ordinary skill in the art would have been motivated to optimize the temperature range by using routine experimentation in order to achieve the desired film roughness and thickness.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the substrate temperature prior deposition of the film, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

11. Claims 1, 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikoma et al., Growth of Si/3C-SiC/Si(100) hetrostructures by pulsed supersonic free jets, *Applied Physics Letters*, Volume 75, No. 25, Pp. 3977-3979, December 1999 in view of Toraguchi et al. (US/6,161,498).

Re claim 1, a method for depositing a thin film, comprising: introducing a gas comprising trisilane to a chamber (see Abstract); wherein the chamber contains a substrate having a predetermined surface are and a substrate surface roughness (see Page 3977, Col. 1); establishing trisilane chemical vapor deposition conditions in the chamber (i.e., CVD chamber See Page 3977, Col. 2) ; and depositing a Si-containing (i.e., Si-C, epi-Si or poly-Si film) film onto the substrate, the Si-containing film having a thickness in the range of 30 – 90 angstroms (i.e., within the overlap claimed range of 10 - 150 angstroms) and a film surface roughness that is greater than the substrate surface roughness by an amount of about 4 angstrom rms (i.e., within the claimed rage of 5 Å rms or less), over a surface area of about 25 micron square (i.e., within the claimed range of one square micron or greater).

However, Ikoma et al. do not specifically disclose using 300 cm^2 or grater wafer (substrate) to deposit the Si-containing film.

Toraguchi et al. disclose utilizing of larger wafer having diameter 300 mm (12 inches), i.e., larger than 300 cm^2 as claimed, in order to deposit thin films for fabrication of IC devices (see Toraguchi et al. Col. 2, lines 24-31; Col. 6, lines 1-13). As known in the art, larger wafer size provides enough surface area to fabricate several hundred individual IC devices on a single substrate assembly and can achieve greater process control and precision in the batch-

processing during fabrication of the semiconductor devices (see Goodman page 1 Paragraph [0005]).

Both Ikoma et al. and Toraguchi et al. teachings are directed to method of fabricating semiconductor devices the method includes utilizing of semiconductor wafer as a base substrate. Therefore, the teachings of Toraguchi et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Ikoma et al. reference with large size wafer i.e., larger that 300 cm^2 size as taught by Toraguchi et al. because larger wafer size provides enough surface area to fabricate several hundred individual IC devices on a single substrate assembly and can achieve greater process control and precision in the batch-processing during fabrication of the semiconductor devices.

Re claim 21, as applied to claim 1above, Ikoma et al. and Toraguchi et al. in combination disclose all the claimed limitation including the limitation wherein establishing trisilane chemical vapor deposition conditions comprises heating the substrate to a temperature in the range of about 700°C to about 900°C in the absence of a plasma (i.e., the temperature of the substrate first stabilized prior growing the film), (i.e., the temperature outside the claimed range of 400°C to about 650°C). Although the combination of Ikoma et al. and Toraguchi et al. temperature is outside of the claimed temperature range that is 400°C to about 650°C, one of ordinary skill in the art would have been motivated to optimize the temperature range by using routine experimentation in order to achieve the desired film roughness and thickness (i.e., the general condition that disclosed by the combination of Ikoma et al. and Toraguchi et al.).

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the substrate temperature prior deposition of the film, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990). Also see MPEP 2144.05.

Re claim 26, as applied to claim 1above, Ikoma et al. and Toraguchi et al. in combination disclose all the claimed limitation including the limitation wherein establishing trisilane deposition conditions comprises maintaining a chamber pressure at predetermined level. Although the combination of Ikoma et al. and Toraguchi et al. do not specifically disclose the chamber pressure range, the claimed pressure that is 1 torr to 100 torr is typical chamber pressure and one of ordinary skill in the art would have been motivated to optimize chamber pressure by using routine experimentation in order to achieve the desired deposition environment (i.e., the general condition that disclosed by the combination of Ikoma et al. and Toraguchi et al.).

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the substrate temperature prior deposition of the film, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed pressure range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

12. Claims 27-29, 31, 33, 36 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US/5,849,601) in view of Toraguchi et al. (US/6,161,498).

Re claim 27, Yamazaki discloses a method for depositing a thin film, comprising: introducing trisilane to a chamber, wherein the chamber contains a substrate having a predetermined surface area; and depositing a continuous amorphous Si-containing film having a thickness of less than about 500 angstroms and a surface area of about one square micron or larger onto the substrate by thermal chemical vapor deposition (i.e., LPCVD that also has heating process) (see Col. 13, lines 5-10).

However, Yamazaki does not specifically disclose using 300 cm^2 or grater wafer (substrate) to deposit the Si-containing film.

Toraguchi et al. disclose utilizing of larger wafer having diameter 300 mm (12 inches), i.e., larger than 300 cm^2 as claimed, in order to deposit thin films for fabrication of IC devices (see Toraguchi et al. Col. 2, lines 24-31; Col. 6, lines 1-13). As known in the art, larger wafer size provides enough surface area to fabricate several hundred individual IC devices on a single substrate assembly and can achieve greater process control and precision in the batch-processing during fabrication of the semiconductor devices (see Goodman page 1 Paragraph [0005]).

Both Yamazaki and Toraguchi et al. teachings are directed to method of fabricating semiconductor devices the method includes utilizing of semiconductor wafer as a base substrate. Therefore, the teachings of Yamazaki and Toraguchi et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Yamazaki and Toraguchi et al. reference with large size wafer i.e., larger that 300 cm^2 size as taught by Toraguchi et al. because larger wafer size provides enough surface area to fabricate several hundred individual IC devices on a single substrate assembly and can achieve greater process control and precision in the batch-processing during fabrication of the semiconductor devices.

In addition, the thickness 100 angstroms or less of the amorphous Si-containing layer can be achieved within the level of ordinary skill in the art in order to optimize the size of the device. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to

choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claims 28 and 29, as applied claim 27 above, Yamazaki and Toraguchi et al. in combination disclose all the claimed limitations including the limitation wherein the substrate comprises a non-single crystal material (i.e., silicon oxide or silicon nitride) (see Yamazaki Fig. 3, Col. Col. 6, lines 12-29).

Re claim 31, as applied claim 27 above, Yamazaki and Toraguchi et al. in combination disclose all the claimed limitations including the limitation wherein the substrate comprises a step or trench (i.e., as depicted in Fig. 3A-3F Yamazaki discloses the substrate 50 comprises a step).

Re claim 33, as applied claim 27 above, Yamazaki and Toraguchi et al. in combination disclose all the claimed limitations including the limitation wherein the depositing is conducted at a temperature in the range of about 450°C – 550°C (i.e. within the claimed range of 450 °C to about 650°C) (see Yamazaki Col. 6, lines 30-35).

Re claim 36, as applied claim 27 above, Yamazaki and Toraguchi et al. in combination disclose all the claimed limitations including the limitation depositing an oxide layer over the Si-containing film (i.e., as depicted in Fig. 3E of Yamazaki, an oxide insulating layer 65 formed over the device that includes Si-containing film) (see Fig 3E and Col. 8, lines 61-67).

Re claim 42, Yamazaki and Toraguchi et al. in combination disclose all the claimed limitations including the limitation wherein the depositing is conducted at a temperature in the range of about 450°C – 550°C (i.e. within the claimed range of 425 °C to about 700°C) (see Yamazaki Col. 6, lines 30-35).

Allowable Subject Matter

13. Claims 55-68, 72-75 will be allowed if the rejection under the judicially created doctrine of obviousness-type double patenting is overcome.

14. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition claims 5-20 also objected as being directly or indirectly depending upon claim 2.

15. Claim 22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition claims 23-25 also objected as being directly or indirectly depending upon claim 22.

16. Claims 30, 32, 34, 37-41 and 43-45, 71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, claim 35 is also objected as

being dependent of claim 34 and claims 44, 45, and 46 also objected as being directly or indirectly depending upon claim 43 respectively.

Response to Arguments

17. Applicants' arguments with respect to claims 1-3, 5-46 and 55-80 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on December 4, 2003.

Remarks

18. Although applicants' argument is consider moot due to the amendment filed on December 4, 2003, as of record, it is respectfully submitted that the teachings of Ikoma et al. is an exemplary and does not limited to deposition of thin films on small wafers is can also be applied to any size of wafer which can be utilized with the type of CVD apparatus that can accommodate the predetermined size of wafer.

Conclusion

19. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 21, 2005
BK

George Fourson
Primary Examiner